IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A method of forming an isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench;

selectively etching a portion of said buffer film layer after the oxide layer has been formed;

applying a layer of isolation material over said buffer film layer~~, with major surfaces of said layer of isolation material and said buffer film layer in contact,~~ and filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

2. (Original) The method of claim 1, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

3. (Previously presented) The method of claim 1, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

4. (Previously presented) The method of claim 3, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

5. (Original) The method of claim 1, further including annealing said isolation material layer.

6-10 (Canceled)

11. (Currently amended) A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:

providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;

etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;

forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;

selectively etching a portion of said buffer film layer after the oxide layer has been formed to expose portions of an upper surface of said dielectric layer adjacent to an upper edge of said trench;

applying a layer of isolation material over said buffer film layer, ~~with major surfaces of said layer of isolation material and said buffer film layer in contact,~~ said isolation material also substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

12. (Original) The method of claim 11, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

13. (Previously presented) The method of claim 11, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

14. (Previously presented) The method of claim 13, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

15. (Original) The method of claim 11, further including annealing said isolation material layer.

16. (Previously presented) The method of claim 11, wherein said capped shallow trench isolation structure includes ledges which extend a distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

17. (Original) The method of claim 16, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.

18-24 (Canceled)

25. (Currently amended) A method of forming an isolation structure on a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench extending through said buffer film layer and said dielectric layer and into said semiconductor substrate, and an oxide layer located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer;

applying a layer of isolation material over said buffer film layer, ~~major surfaces of said layer of isolation material and said buffer film layer in contact,~~ said isolation material substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer; and

removing said buffer film layer.

26. (Previously presented) The method of claim 25, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

27. (Previously presented) The method of claim 26, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

28. (Original) The method of claim 25, further including annealing said isolation material layer.

29-32 (Canceled)

33. (Currently amended) A method of forming a capped shallow trench isolation structure for a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench extending through said buffer film layer and said dielectric layer and into said semiconductor substrate, and an oxide layer located on portions of said semiconductor substrate within said trench, the method comprising:

selectively etching a portion of said buffer film layer to expose portions of an upper surface of said dielectric layer adjacent an upper edge of said trench;

applying a layer of isolation material over said buffer film layer, ~~with major surfaces of said layer of isolation material and said buffer film layer in contact,~~ said isolation material substantially filling said trench;

removing a portion of said isolation material layer above said buffer film layer;

removing said buffer film layer; and

etching said isolation material to form said capped shallow trench isolation structure.

34. (Previously presented) The method of claim 33, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

35. (Previously presented) The method of claim 34, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

36. (Original) The method of claim 33, further including annealing said isolation material layer.

37. (Previously presented) The method of claim 33, wherein said capped shallow trench isolation structure includes ledges which extend a distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

38. (Original) The method of claim 37, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.